

IN THE CLAIMS:

Please revise claims 43 and 66 as indicated below.

1 1. (original claim) Apparatus for deterring failure of a com-
2 puting system; said apparatus comprising:
3 an exclusively hardware network of components, having sub-
4 stantially no software;
5 terminals of the network for connection to such system; and
6 fabrication-preprogrammed hardware circuits of the network
7 for guarding such system from failure.

1 2. (original claim) apparatus of claim 1, particularly for use
2 with such system that is substantially exclusively made up of
3 substantially commercial, off-the-shelf components; and wherein:
4 at least one of the network terminals is connected to
5 receive at least one error signal generated by such system in
6 event of incipient failure of such system; and
7 at least one of the network terminals is connected to
8 provide at least one recovery signal to such system upon receipt
9 of the error signal.

1 3. (original claim) The apparatus of claim 2, wherein:
2 the circuits comprise portions fabrication-preprogrammed to
3 evaluate the at least one error signal to establish charac-
4 teristics of the at least one recovery signal.

1 4. (original claim) The apparatus of claim 1, further
2 comprising:
3 such computing system.

1 5. (original claim) The apparatus of claim 1, wherein:
2 the circuits comprise portions for identifying failure of
3 any of the circuits and correcting for the identified failure.

1 6. (original claim) The apparatus of claim 1, particularly for
2 use with a computing system that has at least one software
3 subsystem for conferring resistance to failure of the system; and
4 wherein:
5 the circuits comprise substantially no portion that in-
6 terferes with such failure-resistance software subsystem.

1 7. (original claim) The apparatus of claim 1, particularly for
2 use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one hardware subsystem for generating a
5 response of the system to failure; and wherein:
6 the circuits comprise portions for reacting to said response
7 of such hardware subsystem.

1 8. (original claim) The apparatus of claim 1, particularly for
2 use with a computing system that has plural generally parallel
3 computing channels; and wherein:

4 the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 9. (original claim) The apparatus of claim 8, wherein:

2 the parallel channels of the computing system are of diverse
3 design or origin.

1 10. (original claim) The apparatus of claim 1, particularly for
2 use with a computing system that has plural processors; and
3 wherein:

4 the circuits comprise portions for identifying failure of
5 any of such processors and correcting for identified failure.

1 11. (original claim) The apparatus of claim 1, wherein:

2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:

5
6 at least three data-collecting and -responding modules,
7 and

8
9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 12. (original claim) The apparatus of claim 1, particularly for
2 use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem for
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 13. (original claim) Apparatus for deterring failure of a
2 computing system; said apparatus comprising:

3 a network of components having terminals for connection to
4 such system; and

5 circuits of the network for operating programs to guard such
6 system from failure;

7 the circuits comprising portions for identifying failure of
8 any of the circuits and correcting for the identified failure.

1 14. (original claim) The apparatus of claim 13, wherein:

2 the program-operating portions comprise a section that
3 corrects for the identified failure by taking a failed circuit
4 out of operation.

1 15. (original claim) The apparatus of claim 14, wherein:

2 the program-operating portions comprise a section that
3 substitutes and powers up a spare circuit for a circuit taken out
4 of operation.

1 16. (original claim) The apparatus of claim 13, further
2 comprising:
3 such computing system.

1 17. (original claim) The apparatus of claim 13, wherein:
2 the program-operating portions comprise at least three of
3 the circuits; and
4 failure is identified at least in part by majority vote
5 among the at least three circuits.

1 18. (original claim) The apparatus of claim 13, particularly
2 for use with a computing system that has at least one software
3 subsystem for conferring resistance to failure of the system; and
4 wherein:
5 the circuits comprise substantially no portion that in-
6 terferes with such failure-resistance software subsystem.

1 19. (original claim) The apparatus of claim 13, particularly
2 for use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one hardware subsystem for generating a
5 response of the system to failure; and wherein:
6 the circuits comprise portions for reacting to said response
7 of such hardware subsystem.

1 20. (original claim) The apparatus of claim 13, particularly
2 for use with a computing system that has plural generally
3 parallel computing channels; and wherein:
4 the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 21. (original claim) The apparatus of claim 20, wherein:
2 the parallel channels of the computing system are of diverse
3 design or origin.

1 22. (original claim) The apparatus of claim 13, particularly
2 for use with a computing system that has plural processors; and
3 wherein:
4 the circuits comprise portions for identifying failure of
5 any of such processors and correcting for identified failure.

1 23. (original claim) The apparatus of claim 13, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:
5
6 at least three data-collecting and -responding modules,
7 and
8
9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 24. (original claim) The apparatus of claim 13, particularly
2 for use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem for
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 25. (original claim) Apparatus for deterring failure of a
2 computing system that has at least one software subsystem for
3 conferring resistance to failure of the system; said apparatus
4 comprising:

5 a network of components having terminals for connection to
6 such system; and

7 circuits of the network for operating programs to guard such
8 system from failure;

9 the circuits comprising substantially no portion that in-
10 terferes with such failure-resistance software subsystem.

1 26. (original claim) The apparatus of claim 25, further
2 comprising:

3 such computing system, including such at least one software
4 subsystem.

1 27. (original claim) The apparatus of claim 25, particularly
2 for use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one hardware subsystem for generating a
5 response of the system to failure; and wherein:
6 the circuits comprise portions for reacting to said response
7 of such hardware subsystem.

1 28. (original claim) The apparatus of claim 25, particularly
2 for use with a computing system that has plural generally
3 parallel computing channels; and wherein:
4 the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 29. (original claim) The apparatus of claim 28, wherein:
2 the parallel channels of the computing system are of diverse
3 design or origin.

1 30. (original claim) The apparatus of claim 25, particularly
2 for use with a computing system that has plural processors; and
3 wherein:
4 the circuits comprise portions for identifying failure of
5 any of such processors and correcting for identified failure.

1 31. (original claim) The apparatus of claim 25, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:
5
6 at least three data-collecting and -responding modules,
7 and
8
9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 32. (original claim) The apparatus of claim 25, particularly
2 for use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem for
6 receiving recovery commands; and wherein:
7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 33. (original claim) Apparatus for deterring failure of a
2 computing system that is substantially exclusively made of sub-
3 stantially commercial, off-the-shelf components and that has at
4 least one hardware subsystem for generating a response of the
5 system to failure; said apparatus comprising:
6 a network of components having terminals for connection to
7 such system; and
8 circuits of the network for operating programs to guard such
9 system from failure;
10 the circuits comprising portions for reacting to said
11 response of such hardware subsystem.

1 34. (original claim) The apparatus of claim 33, wherein:
2 the reacting portions comprise sections for evaluating the
3 hardware-subsystem response to establish characteristics of at
4 least one recovery signal.

1 35. (original claim) The apparatus of claim 34, wherein:
2 the reacting portions comprise sections for applying the at
3 least one recovery signal to such system.

1 36. (original claim) The apparatus of claim 33, further
2 comprising:
3 such computing system, including such hardware subsystem.

1 37. (original claim) The apparatus of claim 33, particularly
2 for use with a computing system that has plural generally
3 parallel computing channels; and wherein:
4 the circuits comprise portions for comparing computational
5 results from such parallel channels.

1 38. (original claim) The apparatus of claim 37, wherein:
2 the parallel channels of the computing system are of diverse
3 design or origin.

1 39. (original claim) The apparatus of claim 33, particularly
2 for use with a computing system that has plural processors; and
3 wherein:
4 the circuits comprise portions for identifying failure of
5 any of such processors and correcting for identified failure.

1 40. (original claim) The apparatus of claim 33, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:
5
6 at least three data-collecting and -responding modules,
7 and
8
9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 41. (original claim) The apparatus of claim 33, particularly
2 for use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem for
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 42. (original claim) Apparatus for deterring failure of a
2 computing system that is distinct from the apparatus and that has
3 plural generally parallel computing channels; said apparatus
4 comprising:

5 a network of components having terminals for connection to
6 such system; and

7 circuits of the network for operating programs to guard such
8 system from failure;

9 the circuits comprising portions for comparing computational
10 results from such parallel channels.

1 43. (currently amended) The apparatus of claim 42, wherein:

2 the parallel channels of such the computing system are of
3 diverse design or origin.

1 44. (original claim) The apparatus of claim 42, wherein:
2 the comparing portions comprise at least one section for
3 analyzing discrepancies between the results from such parallel
4 channels.

1 45. (original claim) The apparatus of claim 44, wherein:
2 the comparing portions further comprise at least one section
3 for imposing corrective action on such system in view of the
4 analyzed discrepancies.

1 46. (original claim) The apparatus of claim 45, wherein:
2 the at least one discrepancy-analyzing section uses a
3 majority voting criterion for resolving discrepancies.

1 47. (original claim) The apparatus of claim 42, further
2 comprising:
3 such computing system.

1 48. (original claim) The apparatus of claim 47, wherein:
2 the parallel channels of the computing system are of diverse
3 design or origin.

1 49. (original claim) The apparatus of claim 48, wherein:
2 the comparing portions comprise circuitry for performing an
3 algorithm to validate a match that is inexact.

1 50. (original claim) The apparatus of claim 49, wherein:
2 the algorithm-performing circuitry employs a degree of
3 inexactness suited to a type of computation under comparison.

1 51. (original claim) The apparatus of claim 49, wherein:
2 the algorithm-performing circuitry performs an algorithm
3 that selects a degree of inexactness based on type of computation
4 under comparison.

1 52. (original claim) The apparatus of claim 42, particularly
2 for use with a computing system that has plural processors; and
3 wherein:
4 the circuits comprise portions for identifying failure of
5 any of such processors and correcting for identified failure.

1 53. (original claim) The apparatus of claim 42, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:
5
6 at least three data-collecting and -responding modules,
7 and
8
9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 54. (original claim) The apparatus of claim 42, particularly
2 for use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem for
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 55. (original claim) Apparatus for deterring failure of a
2 computing system that has plural processors; said apparatus
3 comprising:

4 a network of components having terminals for connection to
5 such system; and

6 circuits of the network for operating programs to guard such
7 system from failure;

8 the circuits comprising portions for identifying failure of
9 any of such processors and correcting for identified failure.

1 56. (original claim) The apparatus of claim 55, wherein:

2 the identifying portions comprise a section that corrects
3 for the identified failure by taking a failed processor out of
4 operation.

1 57. (original claim) The apparatus of claim 56, wherein:
2 the section comprises parts for taking a processor out of
3 operation only in case of signals indicating that the processor
4 has failed permanently.

1 58. (original claim) The apparatus of claim 55, wherein:
2 the identifying portions comprise a section that substitutes
3 and powers up a spare circuit for a processor taken out of
4 operation.

1 59. (original claim) The apparatus of claim 55, further
2 comprising:
3 such computing system.

1 60. (original claim) The apparatus of claim 55, wherein:
2 the circuits comprise modules for collecting and responding
3 to data received from at least one of the terminals, said modules
4 comprising:
5
6 at least three data-collecting and -responding modules,
7 and
8
9 processing sections for conferring among the modules to
10 determine whether any of the modules has failed.

1 61. (original claim) The apparatus of claim 55, particularly
2 for use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem for
6 receiving recovery commands; and wherein:

7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 62. (original claim) Apparatus for deterring failure of a
2 computing system; said apparatus comprising:

3 a network of components having terminals for connection to
4 such system; and

5 circuits of the network for operating programs to guard such
6 system from failure;

7 the circuits comprising modules for collecting and re-
8 sponding to data received from at least one of the terminals,
9 said modules comprising:

10

11 at least three data-collecting and -responding modules,

12 and

13

14 processing sections for conferring among the modules to

15 determine whether any of the modules has failed.

1 63. (original claim) The apparatus of claim 62, further
2 comprising:

3 such computing system.

1 64. (original claim) The apparatus of claim 62, particularly
2 for use with a computing system that is substantially exclusively
3 made of substantially commercial, off-the-shelf components and
4 that has at least one subsystem for generating a response of the
5 system to failure, and that also has at least one subsystem for
6 receiving recovery commands; and wherein:
7 the circuits comprise portions for interposing analysis and
8 a corrective reaction between the response-generating subsystem
9 and the command-receiving subsystem.

1 65. (original claim) Apparatus for deterring failure of a
2 computing system that is substantially exclusively made of sub-
3 stantially commercial, off-the-shelf components and that has at
4 least one subsystem for generating a response of the system to
5 failure, and that also has at least one subsystem for receiving
6 recovery commands; said apparatus comprising:
7 a network of components having terminals for connection to
8 such system between the response-generating subsystem and the
9 recovery-command-receiving subsystem; and
10 circuits of the network for operating programs to guard such
11 system from failure;
12 the circuits comprising portions for interposing analysis
13 and a corrective reaction between the response-generating sub-
14 system and the command-receiving subsystem.

1 66. (currently amended) The apparatus of claim 65 [[2]],
2 further comprising:
3 such computing system.